Gambetti
Vacuum Technology and Related Solutions
Via A. Volta n. 27
20082 Binasco (Milano)
Tel. 39 02 90093082
Fax. 39 02 9052778
info@gambetti.it
www.gambetti.it
www.plasmi.eu

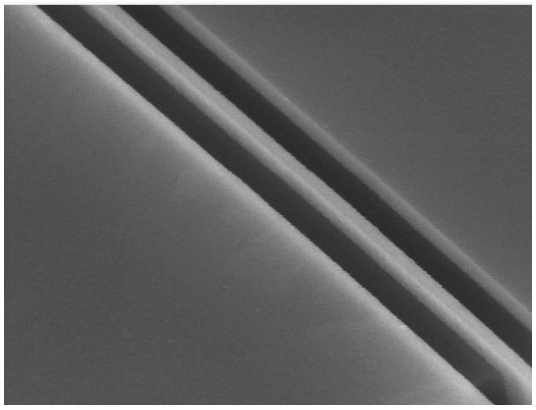
DIMENSIONAL

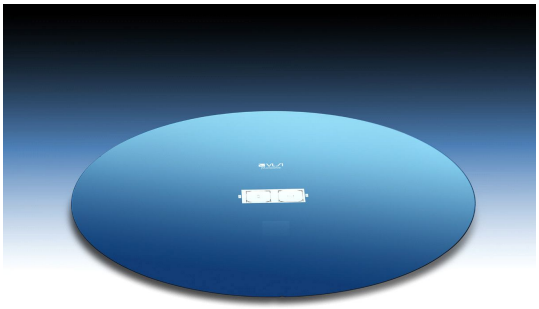
VLSI Standards

NanoCD Standards

IN LINE WITH SUB-100 NM ACCURACY. The NanoCD™ (NCD) is the first commercially available standard to provide line width accuracy calibration at the 45 nm, 90 nm and 130 nm nodes. Use these standards for tool matching, calibrating the width of a CD-AFM tip, or CD-SEM diagnostics.

On the left is an isometric view of a NanoCD 70 nm line, which extends to 3 mm total certified length. At right, the NanoCD is shown mounted into a 300 mm carrier wafer.





PRODUCT DESCRIPTION

The NanoCD consists of a small chip containing a single isolated line 4 mm long (3 mm certified), offering thousands of distinct measurement sites. Chips are fabricated at VLSI Standards using a patented technique that results in lines with high uniformity and low associated uncertainty, unachievable through conventional lithography methods. For compatibility with wafer handlers, the chip is mounted to an etched pocket of a silicon wafer carrier. Global alignment marks, rulers and pattern recognition features extending from the chip to the wafer ensure that the target is always located, and measurements can be repeated.

The width of the line, or the Critical Dimension (CD), is certified with TEM and is traceable to NIST and to the international system of units (SI) through the atomic lattice spacing of single crystal silicon.

PRODUCT SPECIFICATIONS

- **Nominal CD Values**
  25 nm, 70 nm, or 110 nm
- **Accuracy**
  25 nm ± 0.5 nm, 70 nm ± 0.7 nm, 110 ± 0.8 nm
- **Material of CD line**
  Amorphous Silicon
- **Length of Line**
  3 mm certified
- **Defectivity of Line**
  5% Max. (150 µm of total 3,000 µm)
- **Traceability**
  Traceable to the SI units through the atomic lattice spacing in the silicon crystal by TEM
- **SEMI Specification Silicon Wafers**
  200 and 300 mm diameter wafers available in X or X,Y configuration

Revision NCD 061213
Specifications subject to change.

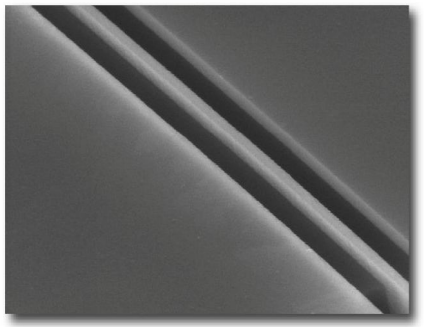
DIMENSIONAL

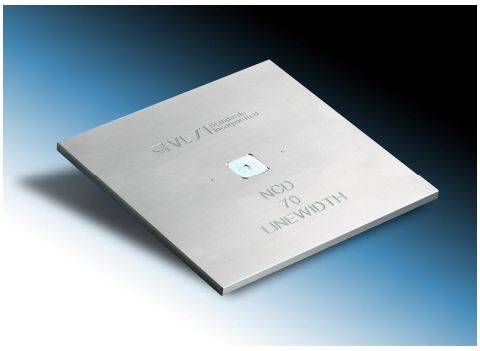
VLSI Standards

NanoCD Standards For Mask Handling Tools

STAY IN LINE WITH SUB-100 NM ACCURACY. The NanoCD™(NCD) is the first commercially available standard to provide line width accuracy calibration at the 130 nm, 90 nm, and 45 nm nodes. Use it for tool matching, calibrating the width CD-AFM tip or diagnostics a CD-SEM, and prevent bias from ever leaving the mask shop.

On the left is an isometric view of a NanoCD 70 nm line, which extends to 3 mm total certified length. At right, the NanoCD is shown mounted into a 6" x 6" x ¼" aluminum carrier, compatible with all reticle loaders and storage.





PRODUCT DESCRIPTION

The NanoCD consists of a small chip containting a single isolated line 4 mm long, offering thousands of disctinct measurement sites. Chips are fabricated at VLSI Standards using a patented technique that results high uniformity and low associated uncertainty lines, unachievable through conventional lithography methods. For compatibility with reticle loaders, the chip is mounted to an aluminum replica of a quartz photomask. Global alignment marks, rulers and pattern recognition features extending from the chip to the reticle ensure that the target is always located, and measurements can be repeated.

The width of the line, or the Critical Dimension (CD), is certified with TEM and is traceable to NIST and to the international system of units (SI) through the atomic lattice spacing of single crystal silicon.

PRODUCT SPECIFICATIONS

- **Nominal Available CD Values**

25 nm, 70 nm, or 110 nm.

- **Accuracy**

25 nm ± 0.5 nm, 70 nm ± 0.7 nm, 110 ± 0.8 nm

- **Material of CD line**

Amorphous Silicon

- **Length of Line**

3 mm certified

- **Defectivity of Line**

5%Max. (150 µm of total 3,000 µm)

- **Traceability**

Traceable to the SI units through the atomic lattice spacing in the silicon crystal by TEM

- **Substrate**

152 mm x 152 mm x 0.25 mm Aluminum.

Specifications subject to change.

Revision MaskNCD061213

3087 North First Street, San Jose, CA 95134-2006 phone 800.228.8574 fax 408.428.9555 www.vlsistandards.com

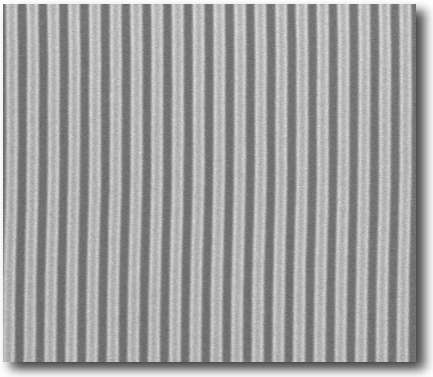
DIMENSIONAL

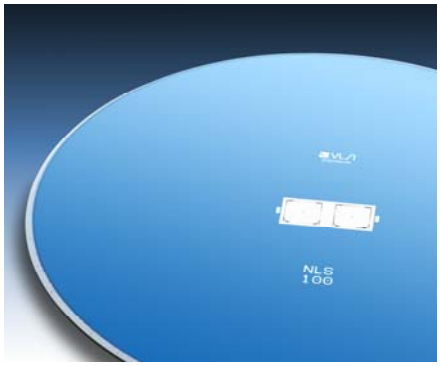
VLSI Standards

Nanolattice Pitch Standard

SET THE SCALE FOR ADVANCED LITHOGRAPHY. The NanoLattice™ (NLSM) 100 nm pitch standard utilizes gratings with near perfect periodicity to calibrate magnification of CD-SEM and Atomic Force Microscopes (AFM). Make the grade, with the only pitch standard of its kind available below the 130 nm node.

On the left is a 2µm FOV CD-SEM micrograph of a NanoLattice Standard in the X configuration. The image on the right shows a 300 mm wafer with optional gratings, mounted in perpendicular XY configurations.





PRODUCT DESCRIPTION

The NanoLattice standard is a 1.2 mm x 1 mm etched silicon grating with a nominal pitch of 100 nm. Each grating is continuous over a large certified area, giving thousands of sites for tens of thousands of measurements. Global alignment marks located 25 mm from the center of wafer on both sides of the chip can be used to assist pattern recognition and automation. Each standard is individually mounted on a carrier wafer, compatible with 200 mm and 300 mm wafer handlers and storage.

PRODUCT SPECIFICATIONS

- **Certified Pitch Values**

100 nm, 200 nm, 400 nm, 800 nm, 1000 nm

- **Uncertainty of 100 nm Pitch Metrology**

< 1 nm

- **Nominal Value**

100 nm ± 2 nm

- **Material**

Silicon <100>

- **Pattern Defect Density**

Less than 1 defect size > 0.2 µm per 50 image frames of size 1.5 µm x 1.5 µm

- **Silicon Die Dimensions**

1.2 mm x 1 mm

- **Certified Area**

800 µm x 800 µm

- **Traceability**

Traceable to SI units through NIST

Specifications subject to change.

Revision NLSM041512

Five Technology Drive, Milpitas, CA 95035-7916 phone 800.228.8574 fax 408.428.9555 www.vlsistandards.com

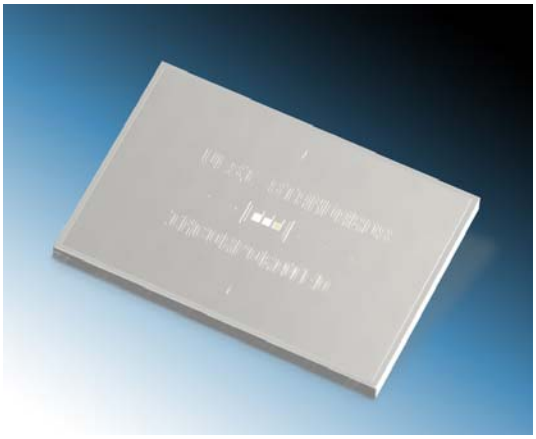
DIMENSIONAL

VLSI Standards

Surface Topography Standards

STAY ON TOP OF 3D PROBE CALIBRATION. The Surface Topography Standard (STS) uses a combination of step height and pitch to enable three-dimensional calibration of optical interferometric microscopes and AFMs. Multiple pitch gratings take calibration further, allowing characterization of scan linearity. On high resolution tools such as the Atomic Force Microscope, traceability to SI units through NIST calibration can be achieved, driving your equipment to its full potential.

The Surface Topography Standard, shown at right, consists of an etched silicon dioxide "waffle pattern" on a silicon substrate.



PRODUCT DESCRIPTION

The Surface Topography Standard consists of a 12 mm x 8 mm silicon die with a pitch cluster patterned in a layer of silicon dioxide. The pitch cluster contains three distinct grid patterns. Each grid pattern measures approximately 270 µm x 270 µm and consists of an array of alternating bars and spaces with an extremely uniform pitch in both the X and Y direction. Two models are available: the STS2 has pitches of 1.8 µm, 3 µm, and 5 µm; the STS3 has pitches of 3 µm, 10 µm, and 20 µm. Each model is available with vertical step heights of either 18 nm, 44 nm, 100 nm or 180 nm. Our precise manufacturing technique ensures a very regular topographic pattern, allowing accurate measurement across the entire working area of the standard.

PRODUCT SPECIFICATIONS

- **Dimensions**
  12 mm x 8 mm silicon die
- **Materials**
  Silicon Dioxide on Silicon coated with Platinum (except STS2-1000S & STS2-1800S models)
- **Nominal Pitch Values (X and Y)**
  STS2: 1.8 µm, 3 µm, and 5 µm (all on one standard)

  STS3: 3 µm, 10 µm, and 20 µm (all on one standard)
- **Nominal Height Values (Z)**
  18 nm, 44 nm, 100 nm, 180 nm
- **Traceability**
  Traceable to SI units through NIST

Revision STS041512
Specifications subject to change.

Five Technology Drive, Milpitas, CA 95035-7916 phone 800.228.8574 fax 408.428.9555

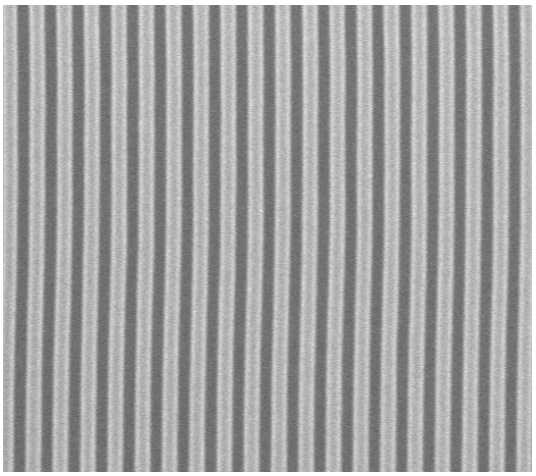
DIMENSIONAL

VLSI Standards

NanoLattice Pitch Standard for Mask Handling Tools

SET THE SCALE FOR ADVANCED LITHOGRAPHY. The NanoLattice™ (NLSM) 100 nm pitch standard utilizes gratings with near perfect periodicity to calibrate magnification and scan linearity of CD-SEM and Atomic Force Microscopes (AFM). Make the grade, with the only pitch standard of its kind available below the 130 nm node.

On the left is a 2µm FOV CD-SEM micrograph of a NanoLattice Standard. The image on the right shows a 6" reticle with optional gratings, mounted in perpendicular XY configurations.



PRODUCT DESCRIPTION

The NanoLattice standard is a 1.2 mm x 1 mm etched silicon grating with a nominal pitch of 100 nm. Each grating is continuous over a large certified area, permitting tens of thousands of measurements. Global alignment marks on both sides of the chip can be used to assist pattern recognition and automation. Each standard is individually mounted on a 6" x 6" x ¼" carrier reticle, compatible all photomask handlers.

PRODUCT SPECIFICATIONS

- **Substrate**
  152 mm x 152 mm x 0.25 mm Al carrier
- **Certified Pitch Values**
  100 nm, 200 nm, 400 nm, 800 nm, 1000 nm
- **Uncertainty of 100 nm Pitch Metrology**
  < 1 nm
- **Nominal Pitch Value**
  100 nm ± 2 nm
- **Material**
  Silicon <100>
- **Pattern Defect Density**
  Less than 1 defect size > 0.2 µm per 50 image frames of size 1.5 µm x 1.5 µm
- **Certified Area**
  800 µm x 800 µm
- **Traceability**
  Traceable to SI units through NIST

Revision MaskNLSM 041512
Specifications subject to change.

Five Technology Drive, Milpitas, CA 95035-7916 phone 800.228.8574 fax 408.428.9555 www.vlsistandards.com

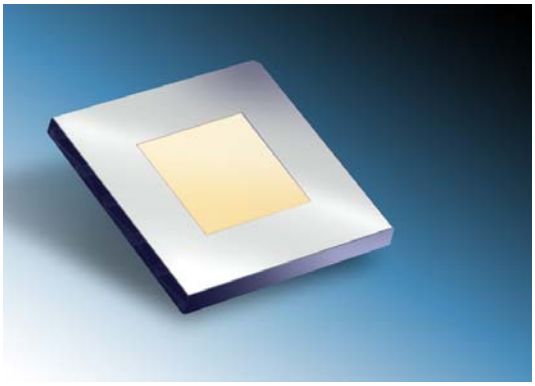
DIMENSIONAL

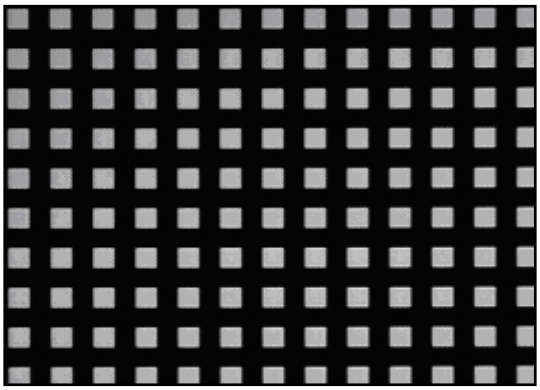
VLSI Standards

Surface Topography References

3D AFM MEASUREMENTS THAT STAND OUT. The Surface Topography Standard (STR) is designed as an auxiliary aid for the monitoring of sophisticated imaging tools such as Atomic Force Microscopes (AFM). The versatile design incorporates features defined in all three spatial directions, allowing correct imaging and the monitoring of the instrument's linearity and long term stability. It also offers valuable information about the piezoelectric functions, sample alignment as well as stylus integrity and condition.

On the left is the picture of a Surface Topography Reference, model STR10. The image on the right shows a top-down view of one of the grid clusters taken with an optical microscope.





PRODUCT DESCRIPTION

The Surface Topography Reference consists of an 8 mm x 8 mm silicon die with a precisely fabricated silicon dioxide pitch cluster. The cluster area is located in the center of the die and contains a grid pattern with a 3 µm pitch in a 1.2 mm x 1.2 mm measurement area (STR3), or 10 µm pitch in a 4 mm x 4 mm measurement area (STR10). The grid pattern consists of an array of alternating bars and spaces with extremely uniform pitch in both the x and y directions. The entire top surface of the die is coated with a very uniform (nominally 40 nm) layer of platinum, making it versatile for both conductive and non conductive probing techniques.

PRODUCT SPECIFICATION

- **Dimensions**
  8 mm x 8 mm silicon die
- **Materials**
  Silicon Dioxide on Silicon coated with Platinum (except 180 nm models)
- **Nominal Pitch Values (X and Y)**
  3 µm, 10 µm
- **Nominal Height values (Z)**
  18 nm, 44 nm, 100 nm, 180 nm
- **Traceability**
  Reference only (not traceable)

Revision STR041512
Specifications subject to change.

Five Technology Drive, Milpitas, CA 95035-7916 phone 800.228.8574 fax 408.428.9555 www.vlsistandards.com

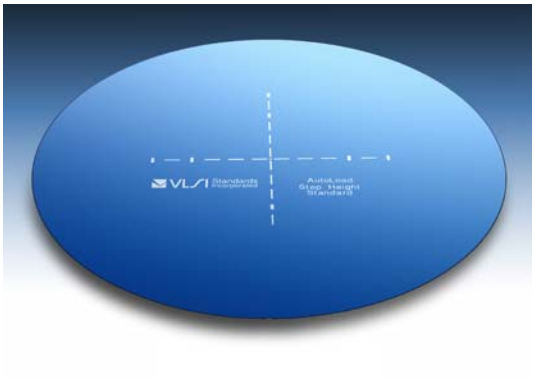
DIMENSIONAL

VLSI Standards

AutoLoad Step Height Standards

TAKING CALIBRATION A STEP FORWARD. The AutoLoad Step Height Standards (ALSHS) are designed for the calibration of surface profilers and Atomic Force Microscopes (AFM) equipped with robotic wafer handling. Intuitive pattern recognition features allow tools to quickly locate the certified feature, measure and acquire step data. When efficiency and performance count, the ALSHS keeps your tool traceable to SI units through NIST, so you can focus on the measurements that matter.

Pictured is a "Thin" AutoLoad Step Height Standard, etched from a 300 mm Oxide film. The certified area is located at the wafer center.



PRODUCT DESCRIPTION

Specifications for Autoload Standards with Steps Smaller than 1 µm:
The "Thin" standard consists of a silicon wafer with a positive step etched out of an oxide film, accommodating of any tip width. The feature is located at the center of the wafer, along with several identical pattern recognition features that can be used for automatically de-skewing wafer rotation, and locating the step height calibration area.

Specifications for Autoload Standards with Steps Larger than 1 µm
For "Thick" steps, the standard consists of a silicon wafer with a negative step etched into the silicon. The feature is located in the center of the wafer, along with several identical pattern recognition features that can be used for automatically de-skewing wafer rotation, and locating the step height calibration area.

PRODUCT SPECIFICATIONS

- **SEMI Specification Silicon Wafers**
  200 mm and 300 mm
- **Available Nominal Step Heights:**
  Thin—8 nm, 18 nm, 44 nm, 88 nm, 180 nm, 450 nm, 940 nm

  Thick—1.8 µm, 4.5 µm, 8.0 µm, 14.5 µm, 19.5 µm, 24 µm, 50 µm, 100 µm
- **Certified Area:**
  Thin—10 µm and 50 µm width

  Thick—1 mm width
- **Traceability**
  Traceable to SI units through NIST Calibrated Specimens, NVLAP accredited

Revision ALSHS041512
Specifications subject to change.

Five Technology Drive, Milpitas, CA 95035-7916 phone 800.228.8574 fax 408.428.9555 www.vlsistandards.com

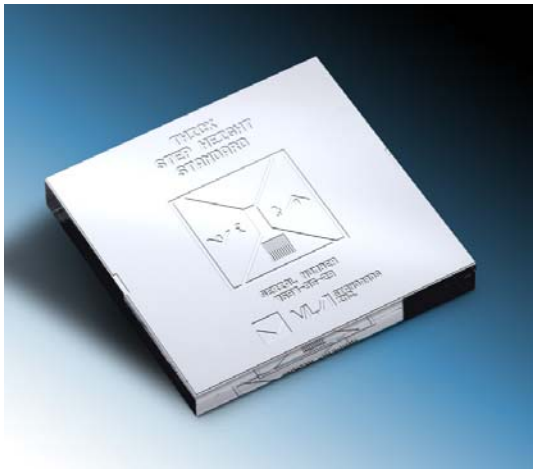
DIMENSIONAL

VLSI Standards

Step Height Standards (Quartz)

TAKING CALIBRATION A STEP FORWARD. Step Height Standards (SHS) are designed to calibrate mechanical or optical surface profilers. These standards consist of a 25 mm x 25 mm x 3 mm quartz block with a precisely etched uniform bar along with various test and diagnostic features. The choice of the material for manufacturing the standard–an ultra smooth quartz photomask blank–assures a very flat and smooth working surface as well as parallelism of the top and bottom surface within a few seconds of arc.

Pictured is a Thick Step Height Standard with chrome coating and showing the step height bar in the center. There are also V-Track and Pitch Array diagnostic tools featured.



PRODUCT DESCRIPTION

Specifications for Step Height Standards with Steps Smaller than 1 µm:
The calibration area of the SHS consists of a positive step 100 µm wide and 750 µm in length and is clearly marked with pointers. The design of this standard incorporates diagnostic features such as incremental pitch for stylus dynamics, size and resolution, a "V" shaped feature for checking stylus integrity, alignment marks, a ruler to facilitate scan length set-up, as well as cross-hair overlay and stylus alignment features. The zoom box and the incremental x, y grid permit determination of the magnification linearity of both optical and mechanical profilers. The standard is coated with a conformal layer of Chromium 90 nm thick to ensure high reflectivity.

Product Description for Step Height Standards larger than 1 µm
The actual calibration area consists of a negative feature (trench) 1 mm wide and 2.5 mm in length and is clearly marked with pointers. Two additional pitch structures form a test track for stylus dynamics and scan speed set-up, while two "V" shaped features can be used to determine the integrity and cleanliness of the stylus. The standard is coated with a conformal layer of Chromium 90 nm thick to ensure high reflectivity.

PRODUCT SPECIFICATIONS

- **Nominal Step Heights:**
  8 nm, 18 nm, 44 nm, 88 nm, 180 nm, 450 nm, 940 nm, 1.8 µm, 4.5 µm, 8.0 µm, 14.5 µm, 19.5 µm, 24 µm, 50 µm
- **Substrate Size**
  25 mm x 25 mm x 3.0 mm
- **Traceability**
  Traceable to SI units through NIST Calibrated Specimens

Revision SHS041512
Specifications subject to change.

Five Technology Drive, Milpitas, CA 95035-7916 phone 800.228.8574 fax 408.428.9555 www.vlsistandards.com

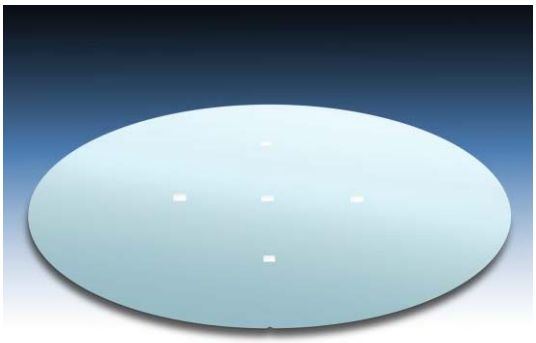
DIMENSIONAL

VLSI Standards

AutoLoad Surface Topography Standards

3D SPM MEASUREMENTS THAT STAND OUT. The AutoLoad Surface Topography Standard (ALSTS) uses a combination of step height and pitch to enable three-dimensional calibration of optical interferometric microscopes and AFMs. Multiple pitch gratings take calibration further, allowing characterization of scan linearity. On high resolution tools such as the Atomic Force Microscope calibration can be achieved driving your equipment to its full potential.

On the left is the Autoload Surface Topography Standard, with 5 distinct pitch clusters.



PRODUCT DESCRIPTION

The ALSTS consists of 5 pitch clusters of varying dimension patterned in a layer of silicon dioxide and coated with Chromium for optimum contrast. The center cluster is certified and traceable to SI units through NIST, while the remaining clusters are for daily use monitors to extend the life of the standard.

Each pitch cluster contains three distinct grid patterns spaced 100 µm apart. Each grid pattern measures approximately 270 µm x 270 µm and consists of an array of alternating bars and spaces with pitch in both X and Y directions. Each model comes standard with 3 pitch clusters, and is available in vertical step heights of either 18 nm, 44 nm, 100 nm, or 180 nm. Our manufacturing technique utilizes advanced lithography methods to obtain a very regular topographic pattern, and statistical sampling to allow accurate measurement Product Specifications across the entire working area of the standard. The Surface Topography Standard is certified and traceable to SI units through NIST for both pitch and step height.

PRODUCT SPECIFICATIONS

- **SEMI Specification Silicon Wafers**
  200 mm and 300 mm
- **Materials**
  Silicon Dioxide on Silicon coated with Chromium
- **Nominal Pitch Values (X and Y)**
  3 µm, 10 µm, and 20 µm (all on one standard)
- **Available Nominal Heights (Z)**
  18 nm, 44 nm, 100 nm, 180 nm
- **Traceability**
  Pitch and Step Height: Traceable to SI units through NIST

Revision ALSTS041512
Specifications subject to change.

Five Technology Drive, Milpitas, CA 95035-7916 phone 800.228.8574 fax 408.428.9555 www.vlsistandards.com

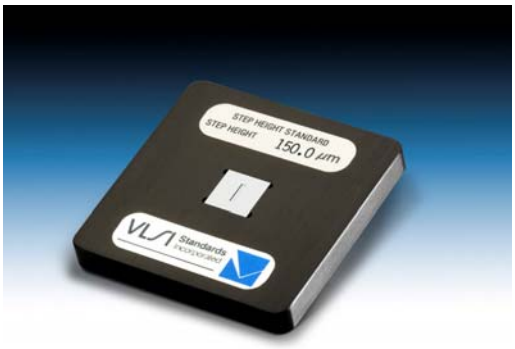
DIMENSIONAL

VLSI Standards

Ultra Thick Step Height Standards (Silicon Die)

TAKE A STEP UP! Ultra Thick Step Height Standards (UTSHS) are designed to calibrate mechanical or optical surface profilers where steps of 100 µm or above are required. These standards consist of a 10 mm x 10 mm silicon die mounted on a 50 mm x 50 mm x 5 mm anodized aluminum substrate.

Pictured is a nominal 150 µm Ultra Thick Step Height Standard.



PRODUCT SPECIFICATIONS

- **Nominal Step Heights:**
  150 µm, 200 µm, and 250 µm
- **Silicon Die Size:**
  10 mm x 10 mm
- **Substrate Size**
  50 mm x 50 mm x 5 mm
- **Uncertainty**
  0.05% or better.
- **Traceability**
  Traceable through PTB
  Calibrated Specimens

PRODUCT DESCRIPTION

The Ultra Thick Step Height Standards consist of a trench etched into a silicon die. The width of the trench is approximately 1 mm. The length of the trench is approximately 4.5 mm. The calibrated area is clearly marked with pointers. The single crystal silicon material that the standard is made of assures a very flat and smooth working surface as well as parallelism of the top and bottom surface. These standards are extremely accurate with a stated 0.05% or better uncertainty. The standard is mounted on an extremely flat, scratch resistant, anodized aluminum substrate.

Revision UTSHS092707
Specifications subject to change.

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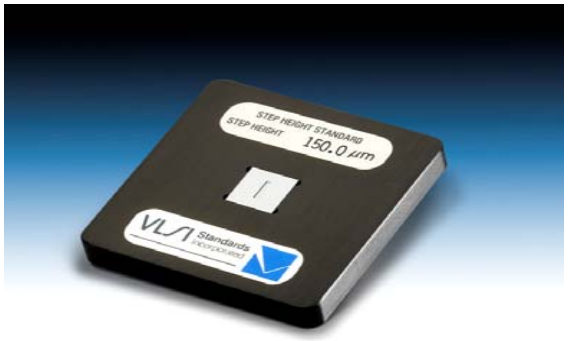

UTSHS Ultra Thick Step Height Standard

Application:	Step Height Calibration
Equipment:	Optical and Mechanical Profiler
Features:	Step height etched into silicon
Traceability:	NIST
Product Range:	150 µm – 250 µm

	Anodized Aluminum Substrate
Step Height (µm)	50 mm x 50 mm x 5 mm
150.0	UTSHS-150
200.0	UTSHS-200
250.0	UTSHS-250

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